

**New generation 2/3", 9.5 Mpix CMOS imager
combines charge-domain global shutter operation
with exceptional high-speed capability**


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Agenda

- Current limitations of 2/3" imagers
 - 4T-4 shared pixel structure
 - Output multiplexer
- New imager overview
 - Improved pixel structure
 - Dual column read out
 - Global shutter operation
 - Serializer and measurement results
 - Detailed imager parameters
- Conclusion

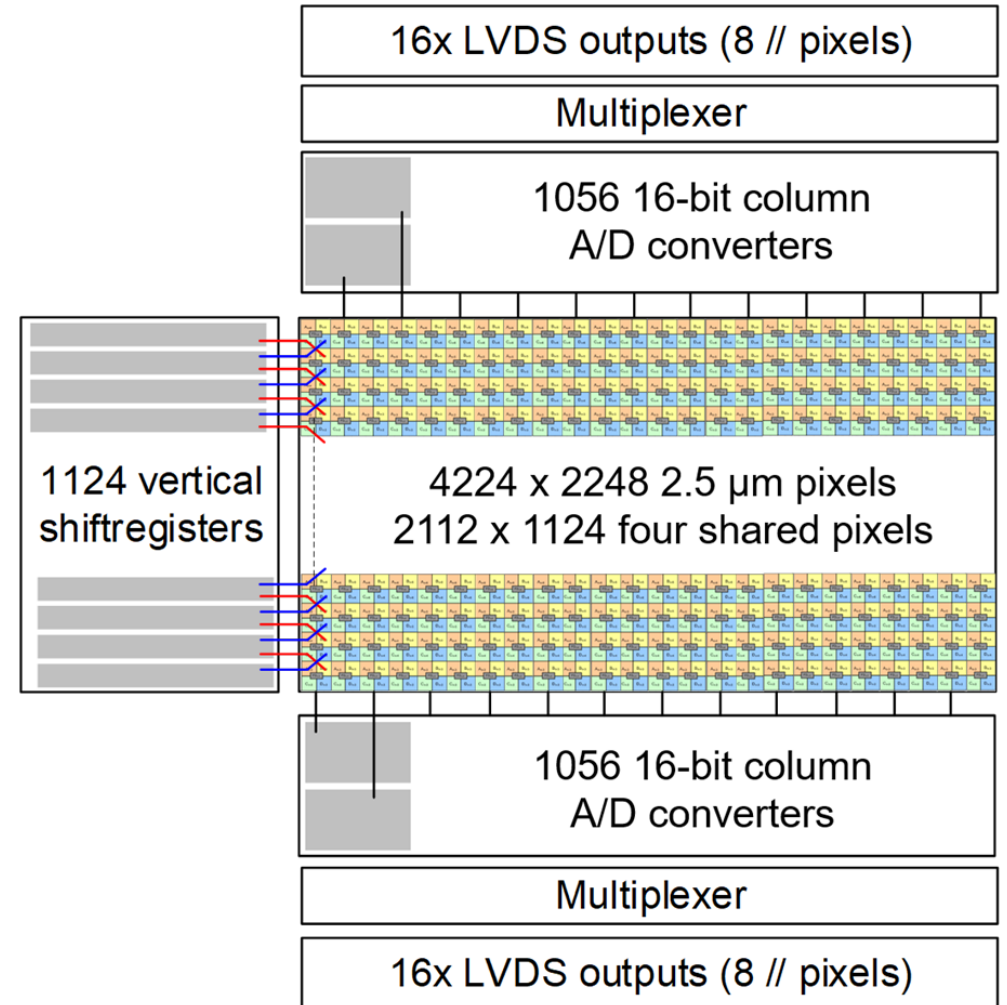
Current Limitations of 2/3" CMOS Imagers with UHDTV-1 Resolution



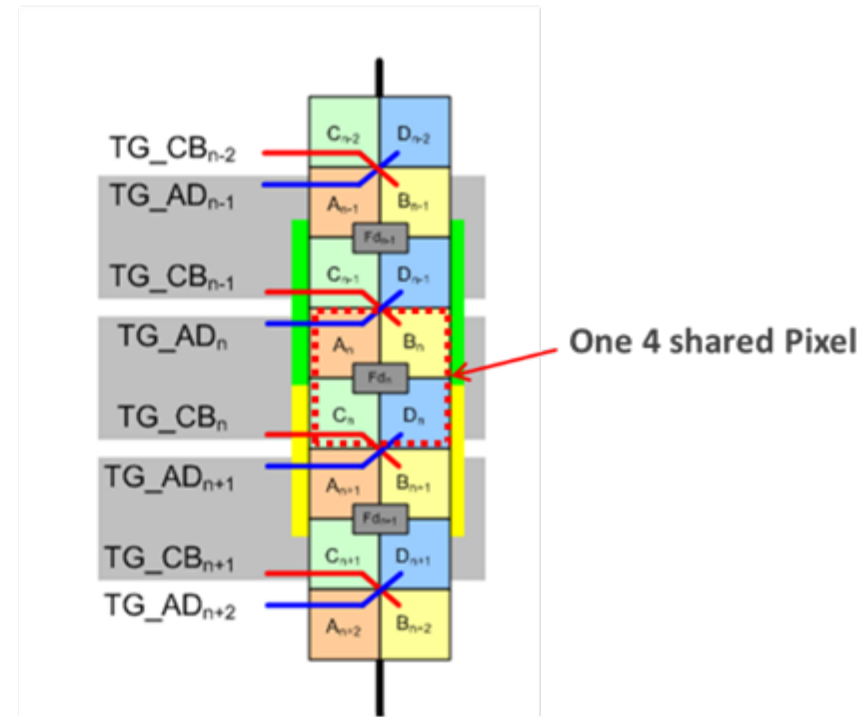
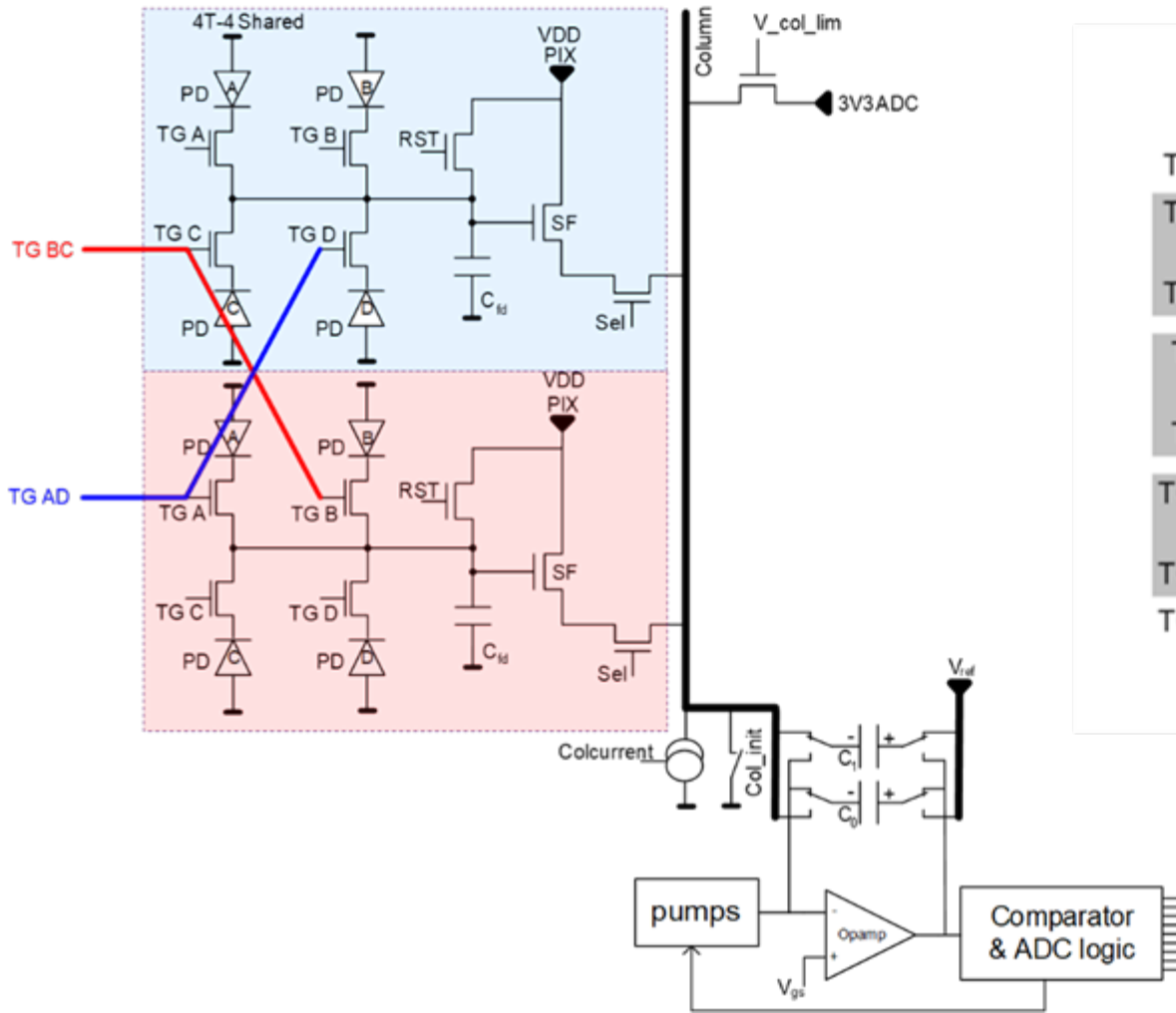
**GAME ON
SMPTE
2020**

**A 2/3" 9.5 Mpixel
CMOS Imager with
High Frame Rate and
HDR Capabilities**

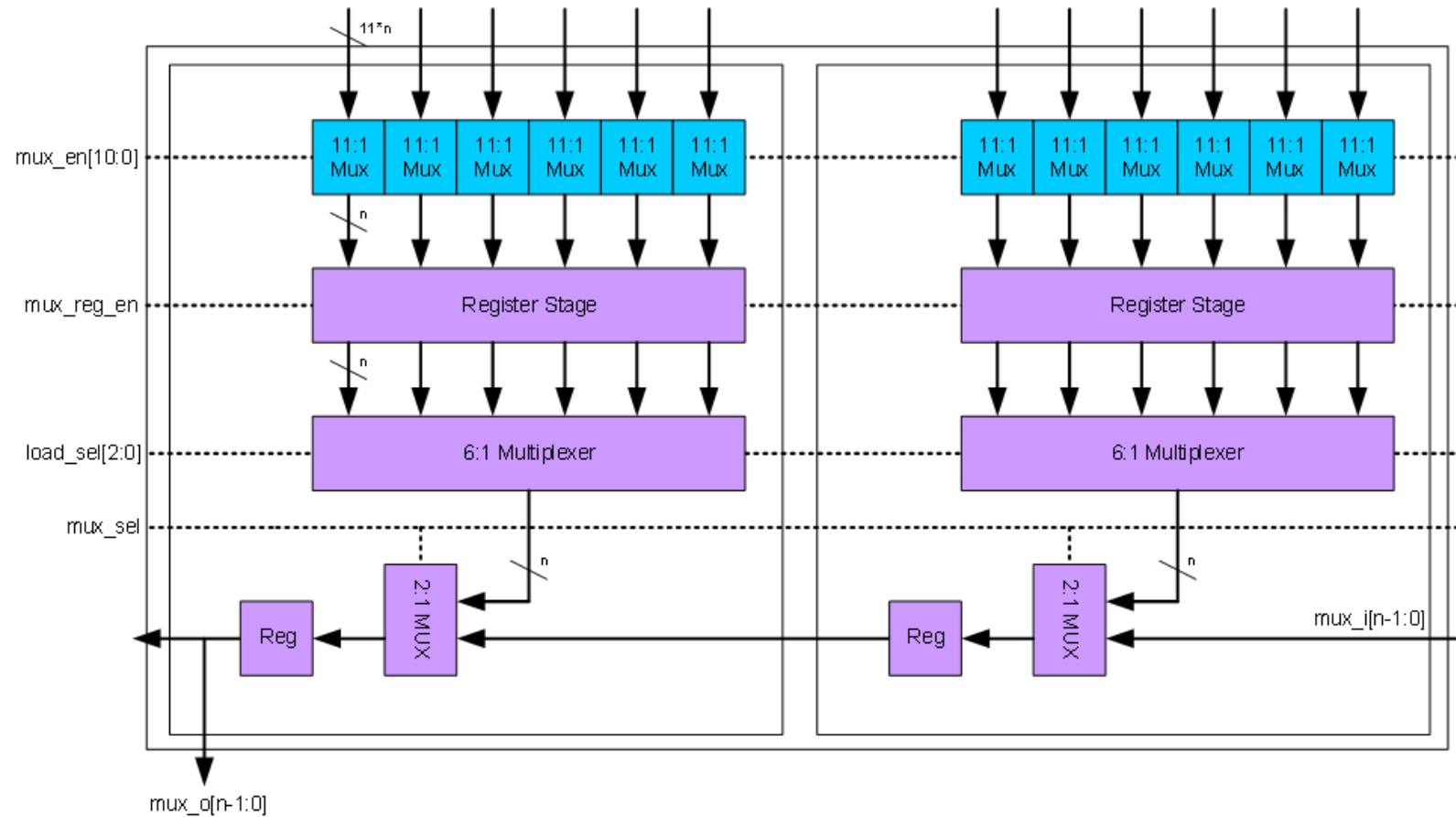
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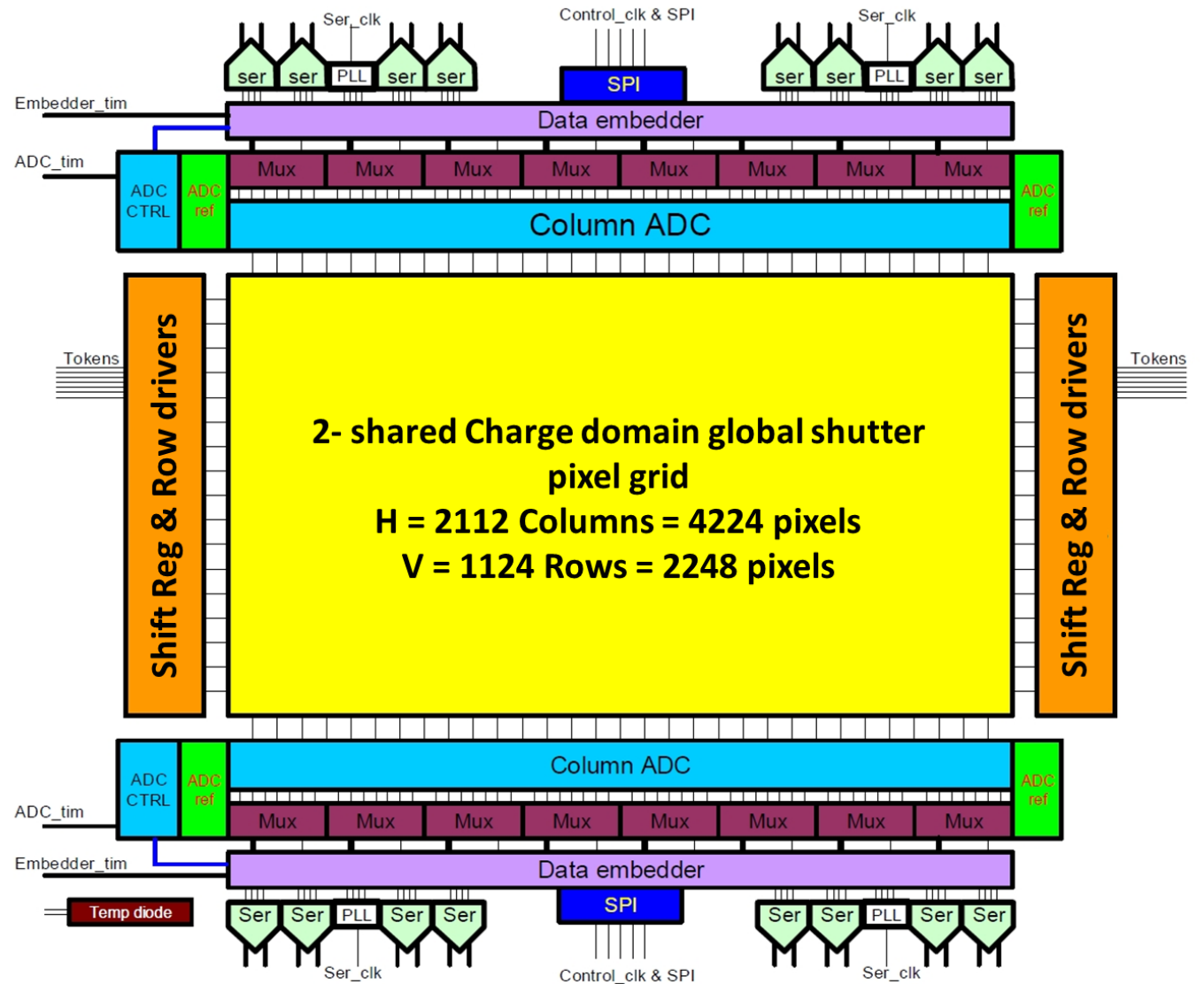
4-shared Pixel Structure



Output Multiplexer



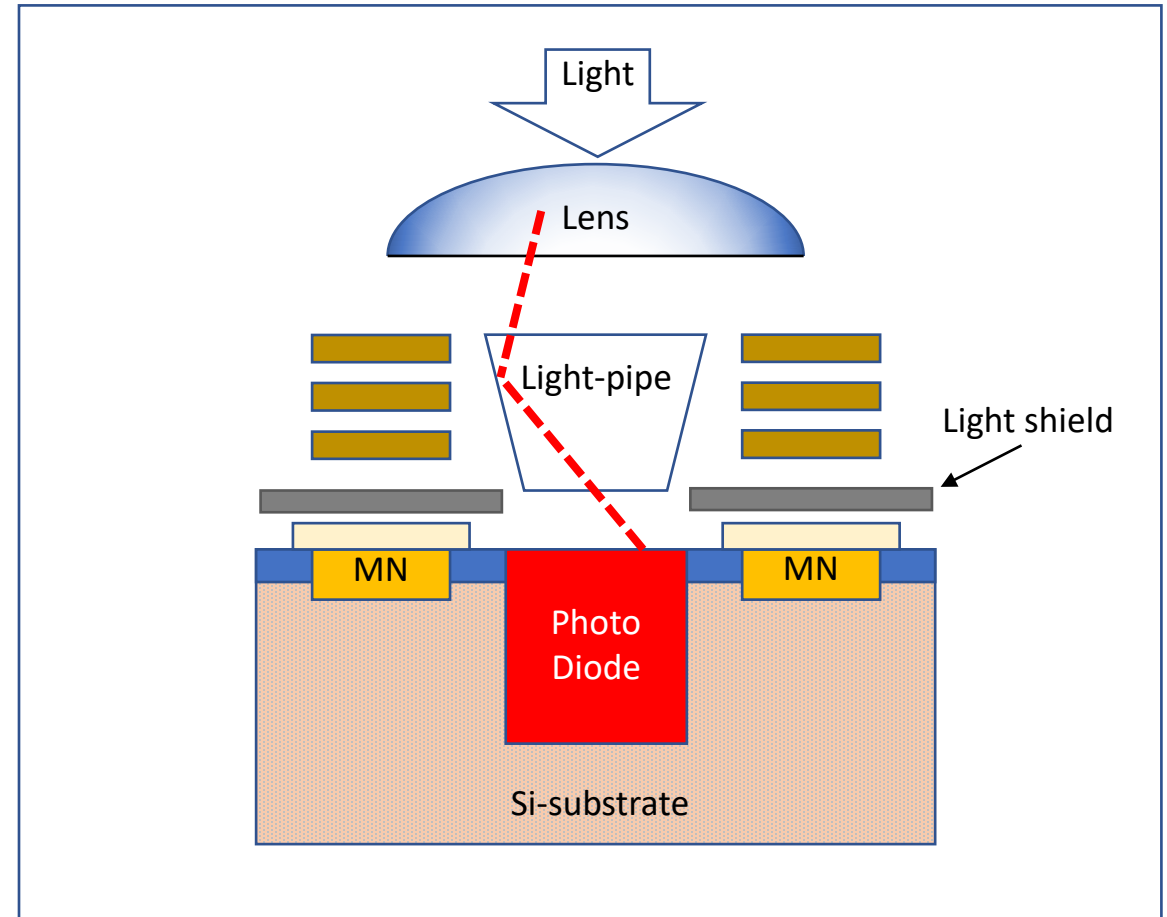
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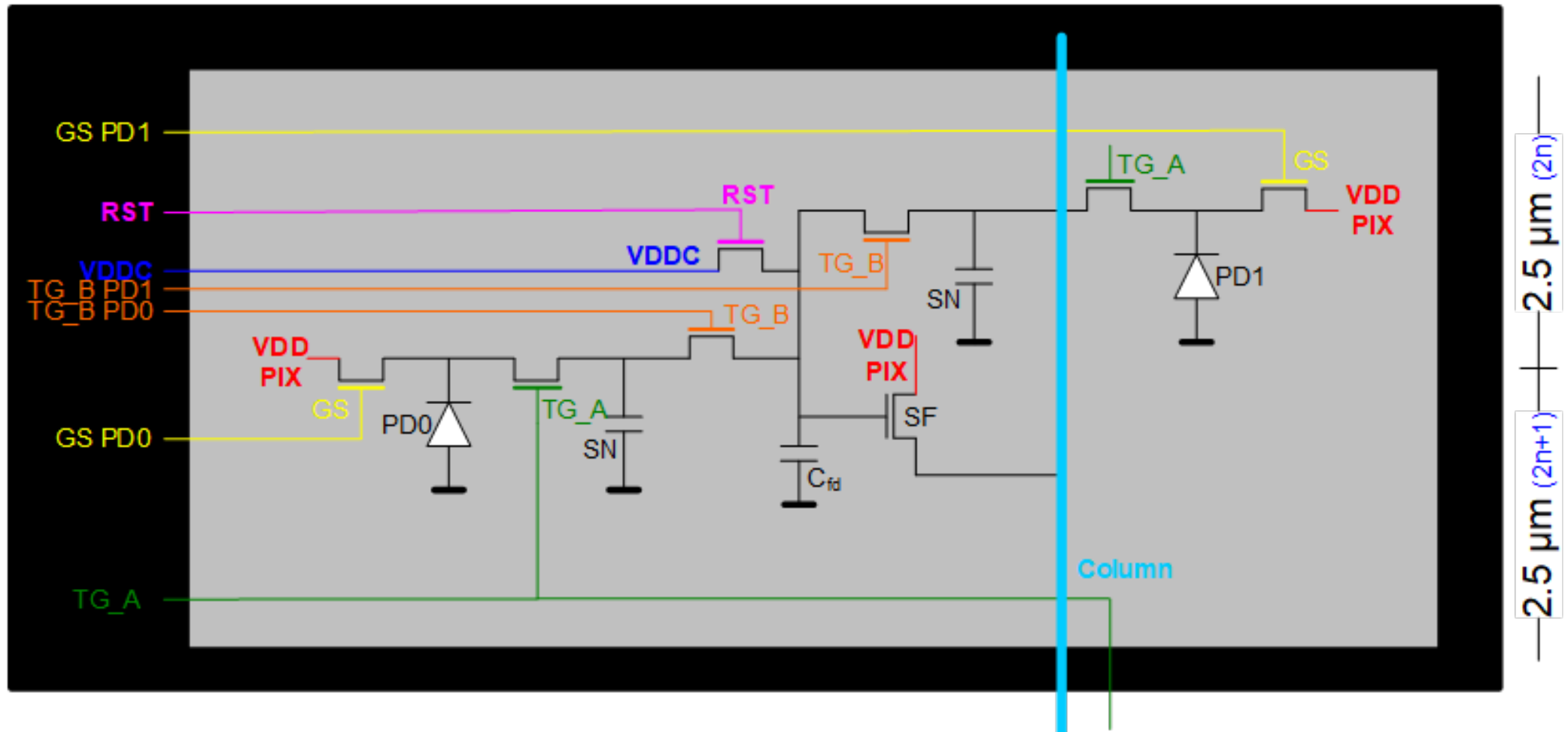
Improved Pixel Structure

65nm CIS process reduces height of the top layer of the imager.
Improved shape of the optical components above the photodiode improves the imager's parasitic light sensitivity (PLS).

Improved PLS delivers better MTF performance.



Selectless 2-Shared Charge Domain Global Shutter Pixel Structure

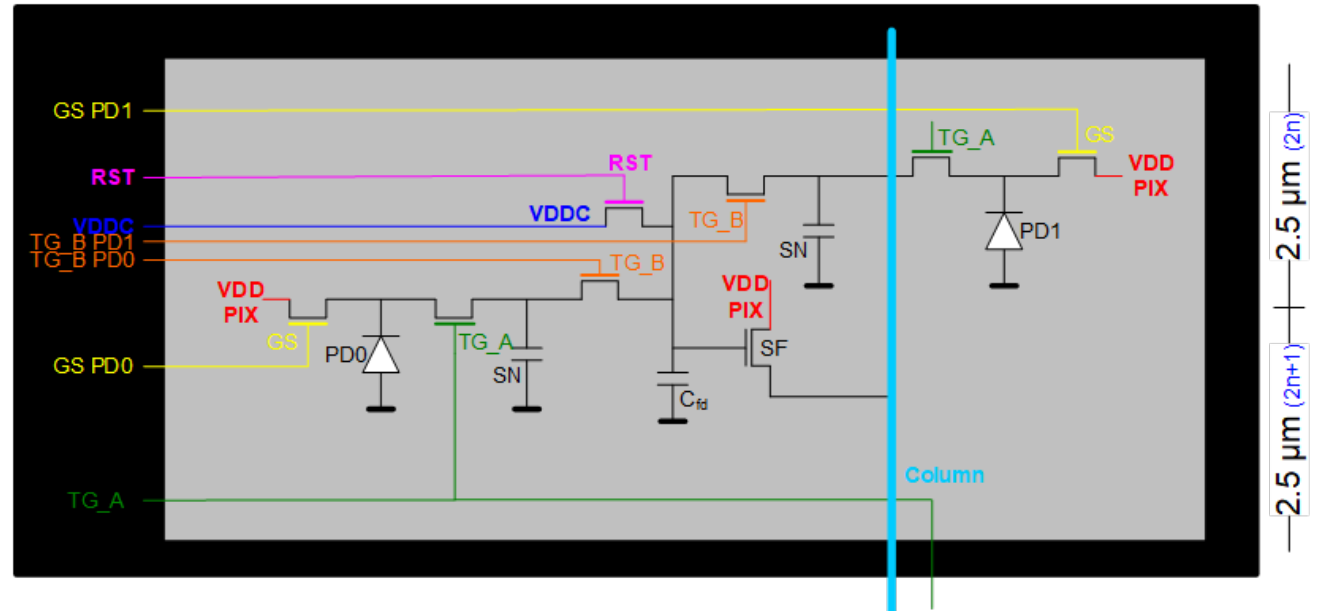


Selectless Pixel

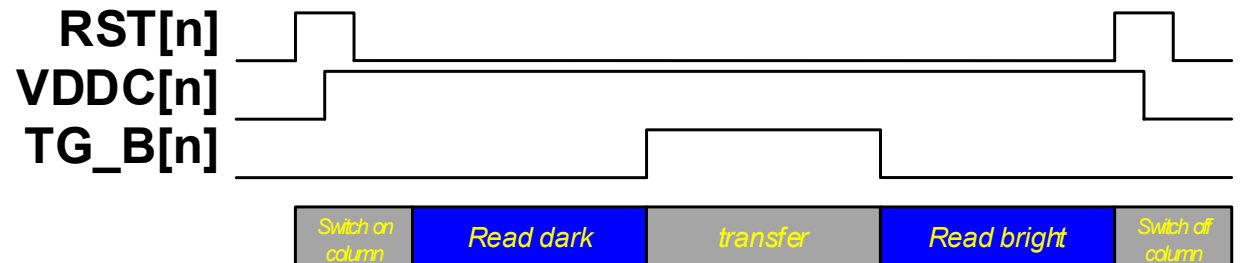
Wait state for column activation
(VDDC/RST)

Wait state for charge transfer from
SN to Cfd (TG_B)

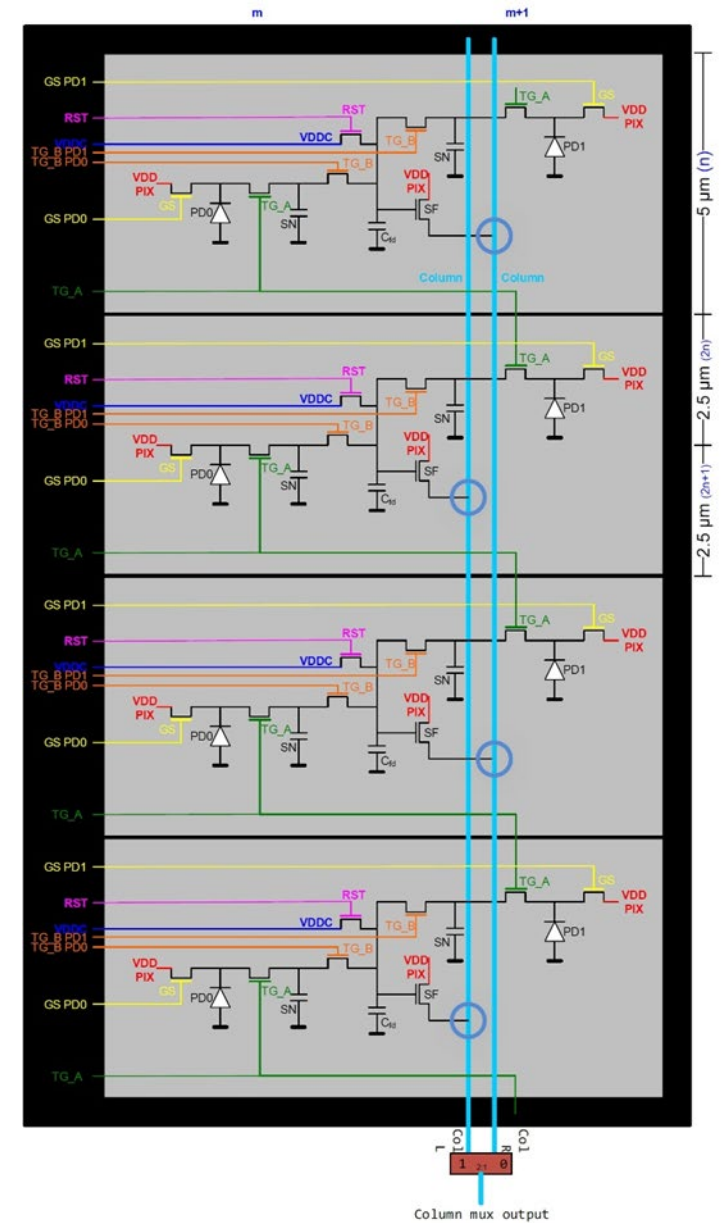
To maximize readout speed the
column should always be read
without waiting for pixel operations.



Conventional timing selectless pixel



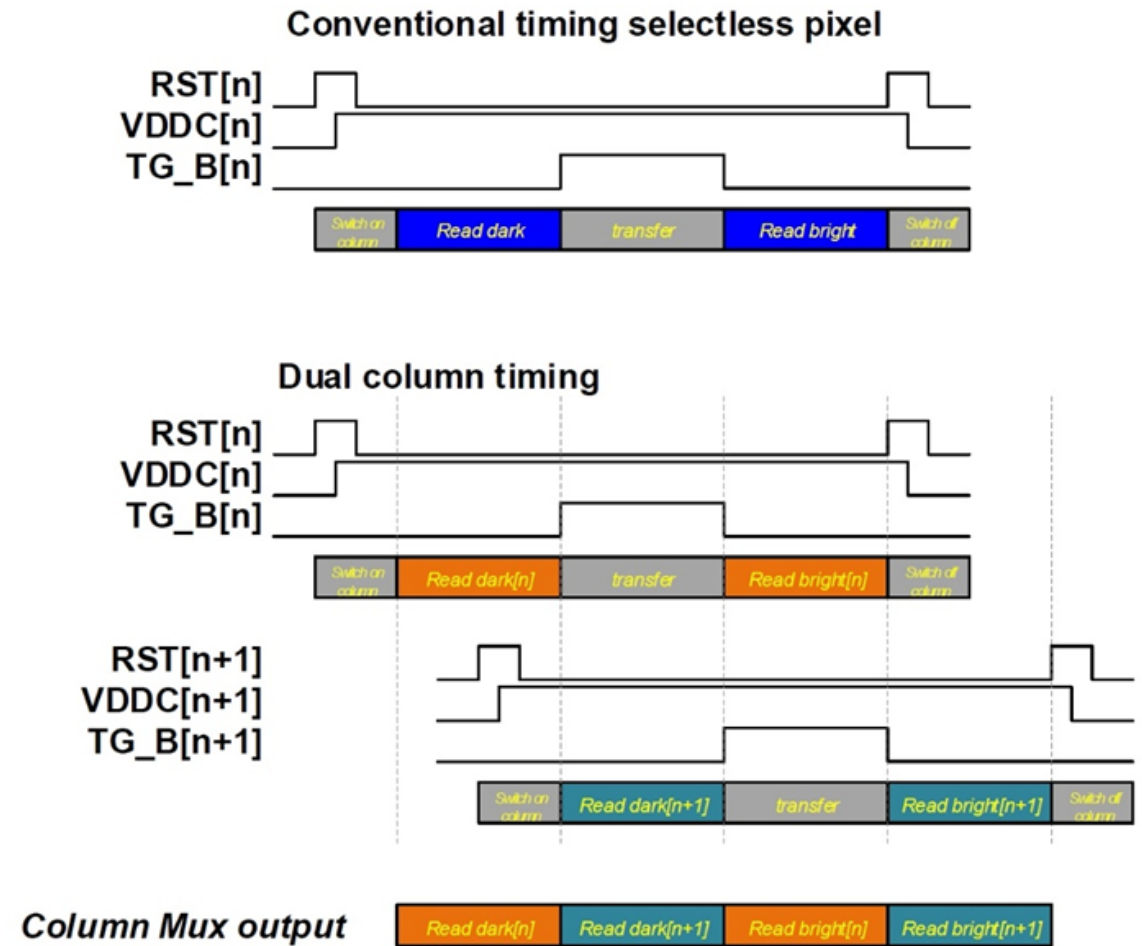
2-shared charge domain global shutter pixel structure with dual column read out



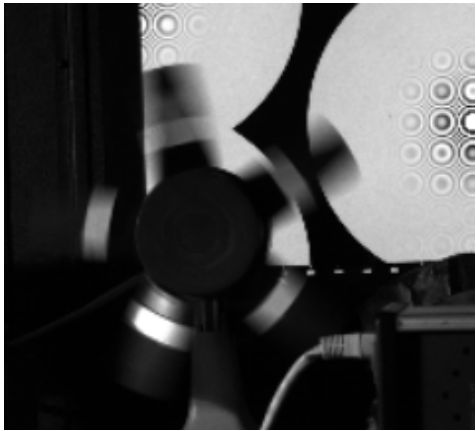
Dual column read out for high frame rate operation

Two rows are operated in parallel to alternate the processes of column sampling, pixel resetting and charge transfer SN to Cfd

Maximizes the throughput of reset- and signal levels out of the pixel array



Global Shutter Operation



Global Shutter



Rolling Shutter

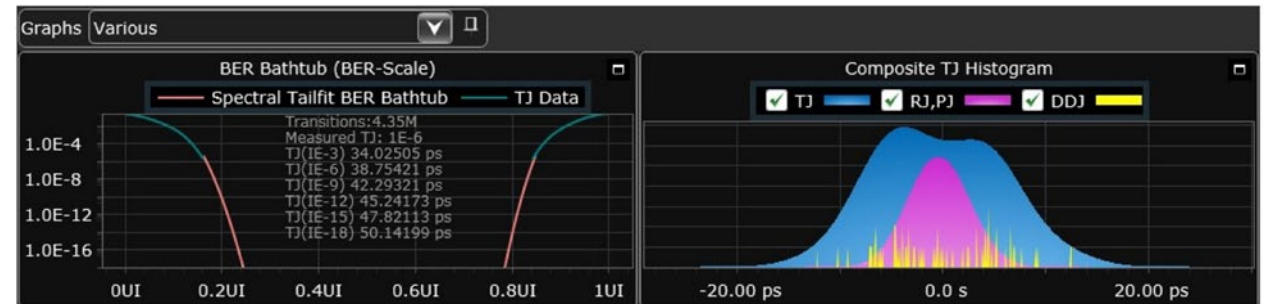
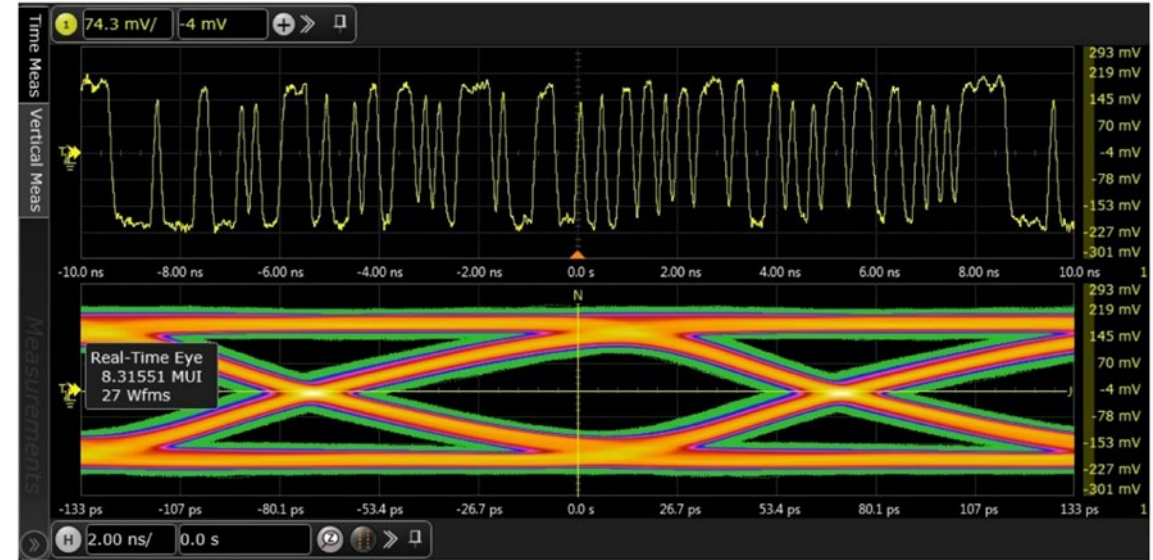


Serializer

The LVDS outputs are replaced by SLVS or scalable low voltage signaling outputs. They provide the same low sensitivity to spurious signals, but reduce the signal swing from 700 mV to 400 mV.

All 16 lanes show similar results with => 7.1 Gbps ok.

Power 8-10 mW/Gbps.



Detailed imager parameters

Native UHD TV-1 pixel count.

Low noise and large full well deliver >15 f-stop of dynamic range.

2112 16-bit A/D converters and 16 SLVS output with 7.2 Gbps each support high speed operation with full resolution.

Parameter	Unit	Value	Note
Resolution	#	4224 (H) x 2248 (V)	9.5 Mpix
Pixel size	μm	2.5	
Shutter type		Global	Charge domain storage
Noise	e^-	1.9	
Full well [e^-]	e^-	7000	
PLS	dB	-80	Typ @ F11
MTF @ 1600 TVL	%	40	
Framerate after CDS	Fps	240	
ADC type		Column wise	Charge based digital multi-slope
ADC count	#	2112	Sum of north and south
ADC noise	μV	120	
ADC resolution	#	14 to 16 bit	240 to 60 Hz framerate
ADC conversion time	ns	<450	
Output interface		SLVS	
# of channels	#	16	
Data rate per channel	Gbps	7.2	
Package		Custom ceramic 215 pin PGA	
Technology node		65 nm, 1P4M	
Die area	mm^2	210	
Control		SPI	
Power	W	1.9 to 3.5	60 to 240 Hz output framerate

Conclusion

We have developed a 2/3" imager for high frame rate UHDTV-1 formats.

To improve image performance, we use charge-domain global shutter pixels with optical components optimized for best PLS/MTF performance.

To achieve high frame rate, we implemented dual columns for parallel line readout and high-speed SLVS outputs that enable 16-bit data samples without compromising pixel performance.

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